4. (Amended) A semiconductor device according to claim 1, further comprising:

at least one adhesion layer formed in an interface between said plurality of wiring lines and said insulating layer, said at least one adhesion layer allowing said plurality of wiring lines and said insulating layer to adhere to one another,

wherein each said at least one adhesion layer has a polishing rate which is essentially equivalent to a polishing rate of said plurality of wiring lines.

Please add the following new claims:

15. (New) A semiconductor device comprising:

a first interlayer insulating layer;

a first layer of low permittivity material formed on said first interlayer insulating layer, said low permittivity material having a property that a migration of copper is limited in said material;

a first plurality of sections of copper being embedded in said first layer of low permittivity material;

a second interlayer insulating layer formed on said layer of low permittivity material,

wherein said first interlayer insulating layer and said second interlayer insulating layer have a property in strength that offsets a property in strength of said first layer of low permittivity material.

16. (New) The semiconductor device of claim 15, wherein said first interlayer insulating layer and said second interlayer insulating layer each comprise SiN, and

said first layer of low permittivity material comprises hydrogen silsesquixane (HSQ).

C3 Cont

17. (New) The semiconductive device of claim 16, further comprising:

a bottom layer formed below said first interlayer insulating layer, said bottom layer having at least one copper conductor line,

wherein said first interlayer insulating layer has a hole formed therein, said hole allowing at least one copper conductor line in said bottom layer to connect with one of said first plurality of sections of copper embedded in said first layer of low permittivity material.

18. (New) The semiconductor device of claim 17, further comprising:

a layer of adhesive material being formed at an interface between said first layer of low permittivity material and each of said first plurality of sections of copper being embedded therein.

19. (New) The semiconductor device of claim 18, wherein said adhesive material comprises tungsten (W).

20. (New) The semiconductor device of claim 15, further comprising:

a third interlayer insulating layer formed on said second interlayer insulating layer;

a second layer of low permittivity material formed on said third interlayer insulating layer, said low permittivity material having a property that a migration of copper is limited in said low permittivity material;

a second plurality of sections of copper being embedded in said second layer of low

permittivity material; and

C3 amK

a fourth interlayer insulating layer formed on said second layer of low permittivity material.

21. (New) The semiconductor device of claim 20, wherein said first interlayer insulating layer, said second interlayer insulating layer, said third interlayer insulating layer, and said fourth interlayer insulating layer each comprising SiN, and

wherein said first layer of low permittivity material and said second layer of low permittivity material each comprises hydrogen silsesquixane (HSQ).

22. (New) The semiconductor device of claim 20, further comprising:

a layer of adhesive material formed at an interface between said second layer of low permittivity material and each of said second plurality of sections of copper being embedded therein.

23. (New) The semiconductor device of claim 22, wherein said adhesive material comprises tungsten (W).

24. (New) The semiconductive device of claim 20, said third interlayer insulating layer has a hole formed therein, said hole allowing a one of said first plurality of sections of copper to connect with one of said second plurality of sections of copper.